REMARKS

A. Status of the Claims and Specification

The Specification was amended for clarity and to correct typographical errors. Claims 1, 2, 3, and 9 have been amended. No new matter has been added. Claims 1–10 remain in this application and are presented for reconsideration.

B. Drawing Objections

The drawings stand objected for failing to comply with the drawing standards set by 37 CFR § 1.84. A Submission of Formal Drawings is filed concurrently herewith, including replacement sheets for FIGS. 1-6. All objections to the drawings are believed to be corrected. No new matter has been added. The removal of the objections to the drawings is respectfully requested.

C. Section 102 Rejection

Claims 1 and 5-10 stand objected under 35 U.S.C. §102(b) as allegedly anticipated by U.S. Patent No. 5,410,490 to Yastrow. In light of the amendments to claims 1 and 9, and the following discussion, Applicants respectfully traverse the rejection.

Referring to the Yastrow reference, disclosed is a method for determining electromigration in a metallic conductor. (Col. 3, lines 15-22). A tool is provided to calculate the average current flow at a node. Next, a minimum metal width for the circuit is determined, where the minimum metal width is sufficient to carry the average current flow. (Col. 5, lines 15-20). Finally, the layout of a circuit is examined to determine if any of the metal layers are deficient based on the minimum width calculation and the current calculation. (Column 3, lines

19-22). The Office contends that the method as disclosed by Yastrow uses a reduced interconnect model because of the limitations of known capacitance extraction programs. (Office Action, page 3). However, using a reduced interconnect model is not equivalent to translating the data to form a model of a circuit interconnect including parasitic electrical properties, nor is it equivalent to obtaining a measure of the performance of the circuit under the influence of the parasitic electrical properties, as expressly as required by the presently claimed invention, as amended.

The present invention, referring to amended claims 1 and 9 and FIG. 5 and supporting text, discloses a method and a computer program for compiling a circuit interconnect model. In particular, the steps required include extracting data from an interconnect (step 515), reading a dataset from the extraction data (step 520), translating the dataset to form a model including parasitic electrical properties (step 535), evaluating the model for a set of conditions to obtain a measure of the performance of the circuit under the influence of the parasitic electrical properties (step 560), and writing the measure of performance to an application (step 580).

The step of translating the dataset to form a model, as recited in amended claims 1 and 9, is included to determine if the dataset read from the extraction data is correct as called upon by an application. If the dataset is not germane, the dataset is translated accordingly. (Specification, page 13, last paragraph). This step is completely absent from Yastrow. Further, Yastrow fails to disclose the step of evaluating the model to determine a measure of performance of the circuit under the influence of the parasitic electrical properties. Even further, Yastrow fails to disclose the step of writing the measure of performance to an application as required by

the present invention. For these reasons alone, claims 1 and 9, and their dependent claims, are patentable over Yastrow. Removal of the § 102 rejection is respectfully requested.

D. Section 103 Rejections

Claims 2 and 4 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Yastrow in view of U.S. Patent No. 6,499,131 to Savithri *et al.* In light of the amendments introduced by this paper, and in light of the following remarks, Applicants respectfully traverse the rejection.

Independent claims 1 and 9 have been amended to clarify the step of reducing the dataset to form a model. Claims 1 and 9 now recite, in part: providing extraction data from an interconnect; reading a dataset from said extraction data from said interconnect; translating said dataset to form a model including parasitic electrical properties; evaluating the model for a set of conditions to obtain a measure of performance of the circuit under the influence of the parasitic electrical properties; and writing the measure of performance to an application..

As noted above, the Yastrow reference fails to disclose all the limitations of independent claims 1 and 9, as amended. The invention of Savithri, while contemplating a method for verification of crosstalk noise, does not supply the features absent from Yastrow. For example, referring to FIG. 7 and supporting text of the Savithri reference, disclosed is a methodology for crosstalk verification including: extracting parasitics from a trial layout of the circuit design (step 701), selecting potential victims and their associated aggressors (step 711), computing crosstalk noise between the victims and their aggressors (step 730), and tabulating the networks with crosstalk noise violations (step 750). (Column 8, line 10 through Column 11, line 31).

However, Savithri fails to disclose translating a dataset to form a model including parasitic electrical properties, and fails to disclose writing the measure of performance (e.g., a set of conditions from the evaluation of a model) to an application as required by the present invention.

In addition, the Office rejects claim 3 under 35 U.S.C. §103(a) as allegedly being unpatentable over Yastrow in view Savithri in further view of U.S. Patent No. 6,522,418 to Yokomizo *et al.* The Yokomizo reference discloses a method and a system for editing images but does not supply the deficiencies of Yastrow and/or Savithri. As such, Applicants traverse the rejection to claim 3 in light of the amendments presented in this paper and the following comments.

The Yokomizo reference discloses a system architecture and method for converting photographic film after exposure to digital data for editorial work. (Column 3, lines 51-63). For example, referring to FIG. 2 of the Yokomizo reference, the method includes: providing undeveloped film to a branch shop, developing the film to obtain photographs, scanning the photographs into digital images, and storing or printing the digital images. (Column 33-40). However, the method of Yokomizo fails to obtain a measure of performance from a model using a view translator. As used herein, the different views of the measure of performance of a circuit interconnect under evaluation do not relate to graphical views, as contemplated by Yokomizo, but rather to different views of the performance of the circuit under evaluation. For example, performance measure views may include distributed parasitics, poles and residues, Elmore delays, PI models and port capacitance. (See, Page 5, lines 11-16). Thus, translating between

different views, as contemplated by the present invention, is completely absent from the proposed combination of Yatrow, Savithi and Yokomizo.

Thus, in light of the claim amendments and the above comments, Applicants believe that claim 1, and its dependent claims, are patentable over the cited references. Applicants respectfully request the withdrawal of the § 103(a) rejections to claims 2, 3, and 4.

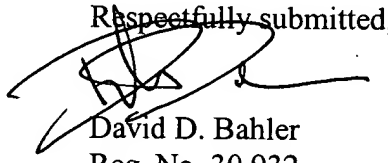
CONCLUSION

Applicants believe the foregoing to be a full and complete response to the subject office action, and respectfully requests the withdrawal of the rejections to claims 1-10 and the issuance of a timely notice of allowance for all of the pending claims.

Should the Examiner believe that a personal discussion would be helpful, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Please date stamp and return the enclosed postcard evidencing receipt of these materials.

Respectfully submitted,



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